LISTING OF THE CLAIMS:

1. (Currently amended) A method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

(a) forming a first polymeric on a surface of a semiconductor wafer having interconnect pads disposed thereon;

(b) patterning said first polymeric material to provide openings that expose said interconnect pads;

(c) forming conductive bump material in said openings;

(d) forming a second polymeric material that is partially cured to a B-stage state ~~over~~ atop said first polymeric material and said conductive bump material;

(e) dicing said semiconductor wafer into individual chips; and

(f) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.

2. (Original) The method of Claim 1 wherein said first polymeric material is formed by a deposition process selected from the group consisting of spin coating, dip coating, brushing, chemical vapor deposition (CVD) plasma-assisted CVD, sputtering, and chemical solution deposition.

3. (Original) The method of Claim 2 wherein said deposition process is spin coating.

4. (Original) The method of Claim 1 wherein said first polymeric material is a dielectric polymeric material selected from the group consisting of polyimides, polyamides, Si-containing polymers, parylene polymers, polybenzocyclobutane and epoxies.

5. (Original) The method of Claim 4 wherein said first polymeric material is an epoxy.

6. (Original) The method of Claim 1 wherein said first polymeric material further includes an inorganic filler.

7. (Original) The method of Claim 6 wherein said inorganic filler is silica, fumed silica, alumina, titanium dioxide, glass fibers or mixtures thereof.

8. (Original) The method of Claim 6 wherein said inorganic filler is present in said first polymeric material in an amount of from about 10 to about 80 wt.%

9. (Original) The method of Claim 1 wherein said first polymeric material has a thickness of from about 25 to about 100 microns.

10. (Original) The method of Claim 1 wherein said wafer is composed of a semiconducting material and has one or more devices present therein.

11. (Original) The method of Claim 1 wherein step (b) includes lithography and etching.

12. (Original) The method of Claim 1 wherein said conductive bump material is solder.

13. (Original) The method of Claim 1 wherein said conductive bump material is applied to said openings by injection molding, evaporation, plating, or a paste screening process.

14. (Original) The method of Claim 1 wherein said second polymeric material is formed by spin coating.

15. (Original) The method of Claim 1 wherein said second polymeric material includes a fluxing agent and an adhesive.

16. (Original) The method of Claim 1 wherein said second polymeric material is a thermoplastic or thermosetting adhesive.

17. (Original) The method of Claim 1 wherein said second polymeric material has a thickness that is thinner than said first polymeric material.

18. (Original) The method of Claim 1 wherein said second polymeric material has a thickness of from about 1 to about 10 microns.

19. (Original) The method of Claim 1 wherein said bonding step occurs a temperature of from about 180° to about 260°C for a time period of from about 1 to about 10 minutes.

20. (Original) The method of Claim 1 wherein said external substrate is a laminate substrate, a chip carrier, a circuit card or a circuit board, each having interconnect pads formed thereon.

21. (Original) A method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

(a) forming a first polymeric material on a surface of a semiconductor wafer having conductive bump material disposed on portions thereof;

(b) removing a portion of said first polymeric material so as to expose top surfaces of said conductive bump material;

(c) forming a second polymeric material on said first polymeric material and said exposed top surfaces of said conductive bump material;

(d) dicing said semiconductor wafer into individual chips; and

(e) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.

22. (Original) The method of Claim 21 wherein step (b) is carried out by polishing or etching.

23-32 (Withdrawn)